Computer Science KS5

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 State what is meant by the term 'register'. A register is a high speed unit of 5 found on the cpu that Stores one piece of data one instruction at a time perform Temporany storage (merrows location One specific purpose Faster alless than RAM / Secondary storage [2] 2. State what is meant by the term-arithmetic logic unit'. The ALU is a register that performs logical and autometic oper ations on data in the CPU, like logical gates (AND, OR, NOT, X DR) addition Studies (AND, OR, NOT, X DR) Conduction Conduction Studies (AND, OR, NOT, X DR) Conduction <	
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auch in the LPU, like logical gates (AND, OR, NUL, 2 DR) and addition	ngage
wit	ith
subtraction results stured in Acc (2) fee	edback
an	าd
	orrect
3. State what is meant by the term control unit.	nswer
Control unit is a vegister that synchronises operations between various Ing	green
registers, sending control signals (memory read, intempts, bus grants)	
along the control bus controls how	
devoted in the CV Bar BPI devote is moved	
and CRUEL MENOY/RAM	
[2]	
Marks are awarded and	
coded feedback is provided.	

Students are encouraged to research and investigate why they did not get full marks for a particular question. After this is completed, the engagement is checked and only then is the mark scheme shared.

ALU, CU, MAR, MOR, PC, AC 5. Describe what happens during the 'Fetch' stage of the Fetch-Decode-Execute cycle.. pc just You should refer to the use of specific registers in your answer. Storag Q In the fetch stage, the address held program counter (PC) the in copied into 15 MAR. memory address register (MAR). the The A memory read signal is sent down the contor bus address stored in 50 the the MAR can travel down the address bus . and The address data stored in the address in MAR is sent down tre data bus and copied into memory data register (MPR); the the RAM value in the PC is incremented by copies data 1 point to the address of the next instruction to fetched be [4] him the Data copied from MDR to CIR Location Describe how the accumulator is used during the Fetch-Decode-Execute cycle. 6. specified by anthemsphie acumulator address bus in stores An the intermedicary result ot on, calculation or onto data bus logical operation performed ŝ the Anthretic Logic Unit (ALU) Students helds all input) output checks to I stores data which Conditional has come from [2] branching MAGI COM 7. Explain which registers and buses are used, and the values they store/carry, when the line LDA first in the LMC program below is executed (after it has been fetched and decoded). You should assume the address first refers to memory location 4. Value from memory copied to MDR into the ACC ("first " location) LDA first ADD second _ value from nevery ("second") copied to MDR - and into -ALL OUT Den with ALV where process occurs HLT first > DAT 15 second DAT 23 held in The value Lose memory location 4 is copied into the pop memory data register via the data bus atter a memory read control signal has been sent across the control kw. This opcode cospect is decoded value held m then loaded accumulator The into the memory location data 5 ts then sent along the address bus into the Memory data register. The value 15 occumbator the copied jato the Anthmetic lugic Unt and value 23 the is copied into the Accumulator -and The "ADD" is an instruction addition. ALU. hence the ope NAC Operand and instruction is copied into the -opeocle-Comment Instruction tas . The value 15 , M ACC Register and decoded Anthrebic is copied into Logic unit and value 23 is oppred into ACC and ALU, where the values are added. The value is loaded back. 1260 ACC and the [6] the MOR for an Memory with larest control signal across control bus and into the value 39 is sont along data bus to be stared in memory weaking, Verbal feedback on topic misconceptions, or exam

technique issues, are provided during lessons.

engage with feedback and correct answer in green